Atomic Clock Aided Receiver for Improved GPS Signal Tracking in the Presence of Wideband Interference

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BIOGRAPHY

Stefan Stevanovic is a PhD candidate at the Navigation Laboratory in the Department of Mechanical and Aerospace Engineering at IIT. He received his B.S. in Mechanical Engineering, and M.S. in Mechanical and Aerospace Engineering, from the Illinois Institute of Technology. His research interests include high accuracy and high integrity navigation algorithms, including fault detection, as well as GPS receiver interference detection and mitigation techniques.

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Dr. Khanafseh is currently a Research Assistant Professor at Mechanical and Aerospace Engineering Department at IIT. He received his M.S. and PhD degrees in Aerospace Engineering from IIT, in 2003 and 2008, respectively. Dr. Khanafseh has been involved in several aviation applications such as Autonomous Airborne Refueling (AAR) of unmanned air vehicles, autonomous shipboard landing for NUCAS and JPALS programs and Ground Based Augmentation System (GBAS). He published 13 journal articles and more than 30 conference papers. His research interests are focused on high accuracy and high integrity navigation algorithms for close proximity applications, cycle ambiguity resolution, high integrity applications, fault monitoring and robust estimation techniques. He was the recipient of the 2011 Institute of Navigation Early Achievement Award for his outstanding contributions to the integrity of carrier phase navigation systems

Dr. Boris Pervan is a Professor of Mechanical and Aerospace Engineering at IIT, where he conducts research on advanced navigation systems. Prior to joining the faculty at IIT, he was a spacecraft mission analyst at Hughes Aircraft Company (now Boeing) and a postdoctoral research associate at Stanford University. Prof. Pervan received his B.S. from the University of Notre Dame, M.S. from the California Institute of Technology, and Ph.D. from Stanford University. He was the recipient of the IIT Sigma Xi Excellence in University Research Award, Ralph Barnett Mechanical and Aerospace Dept. Outstanding Teaching Award, Mechanical and Aerospace Dept. Excellence in Research Award, IIT University Excellence in Teaching Award, IEEE Aerospace and Electronic Systems Society M. Barry Carlton Award, RTCA William E. Jackson Award, Guggenheim Fellowship (Caltech), and the Albert J. Zahm Prize in Aeronautics (Notre Dame). He is an Associate Fellow of the AIAA, a Fellow of the Institute of Navigation (ION), and Editor-in-Chief of the ION Journal Navigation.

ABSTRACT

This work describes a technique for improving the signal tracking performance of stationary GPS receivers that are vulnerable to wideband radio frequency interference (RFI). The method is directly applicable to ground-based reference receivers for differential GPS systems such as the Ground Based and Space Based Augmentation Systems (GBAS and SBAS), as well as other ground-based receivers that require high continuity of service. The high stability of atomic clocks (relative to crystal oscillators) is leveraged to significantly reduce the bandwidth of the receiver phase lock loop (PLL), thereby reducing the impact of wideband interference. The main contribution of this paper is a rigorous theoretical computation and experimental validation of the minimum achievable PLL bandwidth, considering all relevant contributions to phase jitter. The results show that using a rubidium oscillator PLL bandwidths as low as 0.25 Hz are achievable, resulting in reliable tracking at C/No levels as low as 25 dB-Hz. This is 7 dB lower than the 32 dB-Hz standard for GBAS ground stations [4].

Experimental results are then presented to validate the theoretical analysis. The experiments are performed using an RF signal generator to directly simulate a GPS signal with wideband interference, which is realized as a deteriorated carrier-to-noise ratio. The signal generator also reproduces the effects of satellite motion and ionospheric dynamics. The simulated signal enters into a GPS RF front-end kit, which utilizes an external clock input from a commercially available rubidium clock. A software receiver is used for the tracking tests.

I. INTRODUCTION

This work describes a technique for improving the signal tracking performance of stationary GPS receivers that are vulnerable to wideband radio frequency interference (RFI). The method is directly applicable to ground-based reference receivers for differential GPS systems such as the Ground Based and Space Based Augmentation Systems (GBAS and SBAS), as well as other ground-based receivers that require high continuity of service. The high stability of atomic clocks (relative to crystal oscillators) is leveraged to significantly reduce the bandwidth of the receiver phase lock loop (PLL), thereby reducing the impact of wideband interference. The main contribution of this paper is a rigorous theoretical computation and experimental validation of the minimum achievable PLL bandwidth, considering all relevant contributions to phase jitter. The results show that using a rubidium oscillator PLL bandwidths as low as 0.25 Hz are achievable, resulting in reliable tracking at C/No levels as low as 25 dB-Hz. This is 7 dB lower than the 32 dB-Hz standard for GBAS ground stations [4].

The example application considered in this work is GBAS reference station receivers subjected to broadband interference, for example, from nearby use of personal privacy devices (PPDs). Prior work, [9] [10], has shown that PPDs most commonly emit broadband interference, and GBAS ground based reference receivers have experienced tracking discontinuities as a result [1]. These events can cause navigation service interruptions to aircraft on final approach. To ensure continuity of the navigation service GBAS reference stations must be able to track GPS signals in the presence of wideband interference.

Prior research, [5], has capitalized on the idea that reducing the (noise-equivalent) bandwidth of the phase-lock loop (PLL) will reduce the impact of wideband interference. It follows that minimizing the impact of interference requires minimizing PLL bandwidth. However, the bandwidth cannot be reduced significantly using typical TCXO oscillators present in GPS receivers, because of their relatively poor dynamic stability. For this reason, [5] considered atomic clock aiding. Atomic oscillators are more stable, and with recent advancements in technology, chip-scale atomic clocks (CSACs) are now available at a reasonable cost.

This paper goes beyond the fundamental atomic clock aiding ideas presented in [5]. Here the theoretical minimum tracking loop bandwidth is rigorously computed considering all relevant contributions to phase jitter including, thermal noise, satellite and receiver clock jitter, nominal ionosphere, scintillation, and satellite motion. Typically overlooked contributions due to nominal ionosphere and satellite motion become significant at PLL bandwidths below 1 Hz, which are otherwise feasible with atomic clock aiding.

These contributions to phase jitter are evaluated considering a linear model for a standard third-order PLL. A third-order PLL is most frequently used because of its ability to handle dynamics, and additional design freedom compared to a second-order loop. It has zero steady-state error to acceleration stress. However, there will be a steady-state tracking error for jerk stresses.

In this work, the dynamic stresses caused by satellite motion and nominal ionosphere are directly addressed, with the worst-case tracking errors defined by the steady-state errors caused by maximum jerk inputs. For example, to obtain the maximum value of jerk due to satellite motion needed for this computation, satellite motion is simulated over a 24-hour period for a global grid of locations. A similar simulation is used to determine the maximum jerk due to the nominal ionosphere. The International Reference Ionosphere (IRI) 2012 model is used to simulate the slant total electron content (TEC) as a function of time. Finally, other nominal error sources such as thermal noise, and satellite and receiver clock jitter are accounted for in the conventional manner used in [5]. The total variance of phase jitter and dynamic stress error is then used as a performance metric to determine the minimum viable PLL bandwidth.

Experimental results are then presented to validate the theoretical analysis. The experiments are performed using an RF signal generator to directly simulate a GPS signal with wideband interference, which is realized as a deteriorated carrier-to-noise ratio. The signal generator also reproduces the effects of satellite motion and ionospheric dynamics. The simulated signal enters into a GPS RF front-end kit, which utilizes an external clock input from a commercially available rubidium clock. A software receiver is used for the tracking tests. The observed tracking errors are consistent with the theoretically predicted system performance reliable tracking is demonstrated with signal C/No level of 25 dB-Hz using a rubidium oscillator and PLL bandwidth of 0.25 Hz. This C/No level is 7 dB lower than the 32 dB-Hz standard for GBAS ground stations [4]. In addition, it is shown that although the phase jitter metric is a useful design tool, for the bandwidths under consideration the PLL loses lock earlier (i.e. at higher carrier-to-noise ratios) than predicted by the theory. To evaluate experimental results, tracking error variance is used instead, as a more direct metric of continuity of phase lock.

II. LINEAR PLL MODEL

The phase lock loop (PLL) is essentially a feedback control system. A replica carrier signal is created and the PLL attempts to keep its frequency and phase aligned with the incomming carrier signal. More detailed information on the signal processing steps in the PLL is available in [12] [3] [8]. These references actually provide information on the complete GPS signal processing technique, from signal capture at the antenna through pseudorange computation.

For explanation purposes in this paper, the linear PLL model will suffice. The advantage of this model is that it may be analyzed using conventional control system techniques. Figure 1 shows the linear PLL model, where θ is the total phase after down conversion, $\hat{\theta}$ is the generated estimate of θ, and ϕ is the phase error.

The phase error cannot be obtained directly from the PLL. In the non-linear PLL, an estimate of the phase error, called the tracking error ϵ, is obtained by first averaging data samples over T_{CO} seconds, and then passing the result through a phase detector function. As shown in Figure 1, the tracking error ϵ is an estimate of the phase error ϕ corrupted by noise $\tilde{n}$, which is the noise that passes through the phase detector.

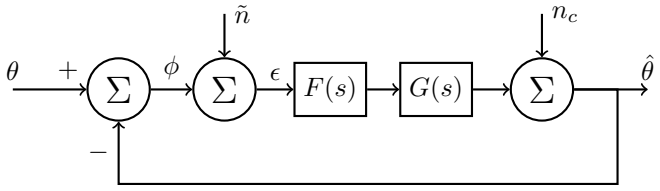

Fig. 1. Linear PLL model including noise sources

This feedback control system model is the result of linearizing the PLL about zero phase error and tracking error, and is assumed to only be valid when the phase error is below a certain threshold, discussed in section III.

The loop filter, $F(s)$, is just a compensator used to achieve desired system response, and it designates the 'order' of the phase lock loop [8]. The numerically controlled oscillator (NCO), $G(s)$, is the plant, which generates the replica carrier signal. The receiver clock is a reference input to the NCO. Therefore, the receiver clock phase noise is modelled as a disturbance, n_c, on the NCO output, as shown in Figure 1.

As shown in the following section, modifying the PLL bandwidth will alter the loop filter transfer function, $F(s)$, to meet certain requirements based on noise performance.

A. Transfer Function for Linear PLL

The closed-loop transfer function of the linear model is given in [5] and is repeated in equation 1. Using $G(s) = 1/s$ for the NCO (because it is an integrator), the input-output transfer function for the system shown in Figure 1 is,

$$H(s) = \frac{\hat{\theta}}{\theta} = \frac{F(s)G(s)}{1 + F(s)G(s)} = \frac{F(s)}{s + F(s)} \tag{1}$$

The complementary, or error transfer function is,

$$H_e(s) = \frac{\phi}{\theta} = \frac{1}{1 + F(s)G(s)} = \frac{s}{s + F(s)} = 1 - H(s) \tag{2}$$

A third-order loop filter is considered in this work because of its ability to handle dynamics, and additional design freedom compared to a second-order loop. It has zero steady-state error to acceleration stress. However, there will be a steady-state phase error for jerk stresses [8]. The transfer function for a third-order loop filter, denoted $F_3(s)$, is,

$$F_3(s) = \frac{b_3 w_{0,3} s^2 + a_3 w_{0,3}^2 s + w_{0,3}^3}{s^2} \tag{3}$$

where a_3, b_3, and $w_{0,3}$ are loop filter coefficients. Typical coefficient values can be found in [8, p. 180; Table 6.5], and values used in this work are discussed in Section II-B.

Substituting equation 3 into system transfer function equations 1 and 2, these transfer functions become,

$$H_3(s) = \frac{F_3(s)}{s + F_3(s)} = \frac{b_3 w_{0,3} s^2 + a_3 w_{0,3}^2 s + w_{0,3}^3}{s^3 + b_3 w_{0,3} s^2 + a_3 w_{0,3}^2 s + w_{0,3}^3} \tag{4}$$

$$H_{3e}(s) = \frac{s}{s + F_3(s)} = \frac{s^3}{s^3 + b_3 w_{0,3} s^2 + a_3 w_{0,3}^2 s + w_{0,3}^3} \tag{5}$$

So, the loop filter coefficients a_3, b_3, and $w_{0,3}$ are chosen based on the design requirements. One design consideration is the equivalent noise bandwidth, often simply refered to as the bandwidth.

B. Noise-Equivalent Bandwidth

The noise-equivalent bandwidth is the "bandwidth of the ideal filter that would pass the same noise power as the filter under study". The noise-equivalent bandwidth expressed in units of Hertz is [12, p. 328, 478, and 485],

$$B_n = \frac{1}{2|H(0)|^2} \int_{-\infty}^{\infty} |H(j2\pi f)|^2 \, df \tag{6}$$

where B_n denotes a one-sided bandwidth, and subscript n means that it is the noise-equivalent bandwidth.

Equation 6 specifies the relationship between the bandwidth and loop filter coefficients. For example, a first-order loop has a single loop filter coefficient. Satisfying a bandwidth requirement would allow that single coefficient to be computed using equation 6, thereby completing the loop filter design. Second and third order loop filters offer additional design freedom. For a third-order loop, two loop filter coefficients in addition to the bandwidth must be specified. The third-order loop filter coefficients used in this work are,

$$a_3 = 1.1 \tag{7}$$

$$b_3 = 2.4 \tag{8}$$

$$w_{0,3} = 0.7845 B_n \tag{9}$$

where, a_3 and b_3 are chosen to be the typical third-order loop filter coefficients specified in [8, p. 180; Table 6.5]. Equation 9 is the result of using equations 7 and 8 in equation 6. The reason typical values for a_3 and b_3 are used is because the focus of this work is to investigate the advantage of using an atomic oscillator on the ability to reject noise by tightening PLL bandwidth. The focus is not controller design.

III. PERFORMANCE METRIC

A conservative and commonly used metric for analyzing tracking performance in the presence of dominant sources of error is often referred to as the total phase jitter rule. This rule can be expressed (in units of degrees) as [8, p. 184],

$$\sigma_{PLL} = \sigma_\phi + \theta_e/3 \leq R \quad \text{deg.} \tag{10}$$

where σ_{PLL} is the total phase jitter, σ_ϕ is the standard deviation of phase jitter (from all sources, including clocks

and thermal noise), θ_e is the tracking error caused by dynamic stresses, and R is the jitter threshold value. This threshold is typically given a value of 15 degrees, beyond which the assumption of PLL linearity is questionable. [8].

In fact, based on an empirical study it has been shown in [13] that the choice of threshold will affect the mean time to lose lock (i.e. mean time between cycle slips). This would interrupt the continuity of navigation service. Therefore, the choice of threshold is critical to maintain a robust system, as we desire in this work.

A. Jitter Threshold

The nominal threshold for phase jitter is 15 degrees. However, for higher order PLLs (i.e. 2nd, and 3rd order), there is a problem. Their mean time to lose lock is shorter than a first order PLL by an order of magnitude [13]. Table I (taken from [13]) shows the mean time to loss of lock for a first order PLL compared to a 3rd order, for total phase jitter of 9-12 degrees.

σ_ϕ [deg.]	1st order PLL [hrs]	3st order PLL [hrs]
9	14149.57	141.50
10	303.02	3.03
11	17.68	0.18
12	2.04	0.02

TABLE I
MEAN TIME TO LOSE LOCK (TAKEN FROM [13])

Based on these results, in this work, 10 degrees is used as the threshold value, R, in equation 10. However, this choice does not affect the methods developed in the remainder of the paper.

Nominal phase jitter contributions are discussed in Section IV, and dynamic stresses are introduced in Section VI.

IV. NOMINAL CONTRIBUTIONS TO PHASE JITTER

Nominal contributions to phase jitter typically include satellite and receiver clock errors, and thermal noise. The variance of phase jitter, σ^2_ϕ, for a stationary receiver is defined as [6] [5],

$$\sigma^2_\phi = \sigma^2_{\phi,\tilde{n}} + \sigma^2_{\phi,\text{clk}} \tag{11}$$

where, $\sigma^2_{\phi,\tilde{n}}$ represents the variance of phase jitter due to receiver thermal (white) noise, and $\sigma^2_{\phi,\text{clk}}$ represents the variance of phase jitter due to SV and receiver clock instabilities.

The contribution due to input white noise, $\sigma^2_{\phi,\tilde{n}}$, is derived in [7] for the Costas discriminator as,

$$\sigma^2_{\phi,\tilde{n}} = \frac{B_n}{(C/N_0)}\left[1 + \frac{1}{2T_{CO}(C/N_0)}\right] \quad [\text{cycles}] \tag{12}$$

where, B_n is the single sided PLL bandwidth, C/N_0 is the carrier-to-noise ratio, and T_{CO} is the coherent integration time (assumed 1ms in this work, unless otherwise stated).

The phase noise due to oscillator instabilities, $\sigma^2_{\phi,\text{clk}}$, is split into components due to satellite and receiver clocks as,

$$\sigma^2_{\phi,\text{clk}} = \sigma^2_{\phi,n_{sv}} + \sigma^2_{\phi,n_c} \tag{13}$$

with,

$$\sigma^2_{\phi,n_{sv}} = \int_0^\infty |H_e(j2\pi f)|^2 S_{sv}(f)\, df \tag{14}$$

$$\sigma^2_{\phi,n_c} = \int_0^\infty |H_e(j2\pi f)|^2 S_{rx}(f)\, df \tag{15}$$

where, $S_{sv}(f)$ and $S_{rx}(f)$ are the single-sided phase error power spectral densities (PSD's) for the satellite and receiver clocks respectively [6].

V. RECEIVER CLOCK COMPARISON

Clock phase error PSD, needed for satellite and receiver clocks in equations 14 and 15, is modelled using a power law as [5] [12],

$$S(f) = h_0 f^0 + h_1 f^1 + h_2 f^2 + h_3 f^3 + h_4 f^4 \tag{16}$$

where h coefficients for several common crystal and atomic oscillators are given in Table II. Power law coefficents for the temperature compensated crystal oscillator (TCXO) and oven controlled crystal oscillator (OCXO) are taken from [12], while the chip-scale atomic clock (CSAC) and rubidium atomic clock coefficients are obtained from [5].

	TCXO	OCXO	CSAC	Rubidium
h_0	5.0×10^{-8}	5.5×10^{-8}	5.0×10^{-8}	5.0×10^{-8}
h_1	6.2×10^{-5}	5.0×10^{-5}	6.2×10^{-5}	6.2×10^{-5}
h_2	9.6×10^{-4}	6.5×10^{-4}	1.6×10^{-6}	5.3×10^{-8}
h_3	6.0×10^{-3}	9.0×10^{-7}	2.9×10^{-10}	0
h_4	6.0×10^{-4}	1.0×10^{-7}	6.1×10^{-12}	1.2×10^{-17}

TABLE II
CLOCK PSD COEFFICIENTS

The phase error power spectral densities (PSDs) for these clocks are shown in Figure 2. Since commercial atomic oscillators typically operate by disciplining a crystal oscillator using the atomic transition frequency of rubidium or cesium, their PSD's coincide at high frequencies. That is, over short time intervals, and atomic oscillator is no more stable than the crystal oscillator used in its design. However, for lower frequencies (or longer time periods) the atomic clocks are more stable because their internal crystal oscillator is corrected or disciplined using the atomic transition frequency.

Prior work [6] [14] has used very conservative methods to compute power law model h coefficients for space vehicle (SV) clocks. The authors essentially shifted the TXCO PSD curve such that it passes through a single point specified by the GPS Standard Positioning Service (SPS) document [11]. The result is a PSD curve that completely bounds that of the TCXO clock. This is extremely conservative considering

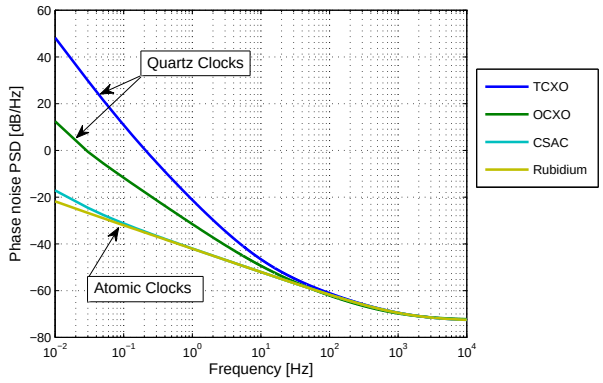

Fig. 2. Receiver Clock Comparison

that satellites are equipped with rubidium (or cesium) atomic oscillators [11]. They divided the resulting PSD by a factor of 100 to reduce the conservatism. However, this would create a PSD which is lower than the TCXO/OCXO PSD for high frequencies. This is not a realistic PSD curve because, as previously discussed, atomic oscillators operate by disciplining a crystal oscillator.

Since GPS satellites (SVs) are equipped with either ceisium or rubidium atomic clocks, it is assumed that the SV clocks have a PSD representative of a rubidium atomic oscillator.

Atomic oscillators are considered for use as reference oscillators for receivers because they are becoming increasingly affordable, and compact. Even though this work focuses on stationary users, chip scale atomic clocks (CSACs) are available, and well suited for mobile navigation applications. The advantage of using atomic oscillators at the receiver is that their lower phase noise at low frequencies compared to crystal oscillators, helps reduce the impact of receiver clock on the variance of phase jitter, σ_ϕ^2.

A. *Effect of Clock Stability on Phase Jitter*

To explain the advantage of atomic oscillators over crystal oscillators, consider Figure 2 and equations 14 to 15. The complementary transfer function $H_e(j2\pi f)$ is a high-pass filter. Now, as a simple example, imagine that it is an ideal high-pass filter with a 10 Hz bandwidth. This means it will pass all frequencies greater than 10 Hz with unit gain. Equations 14 and 15 then reduce to simply the integral of the PSD with limits of integration from 10 Hz to infinity. Now, referring to Figure 2 it is clear that for frequencies greater than 10 Hz, the PSDs for crystal oscillators and atomic clocks are nearly identical. Therefore, this exercise concludes that for a 10 Hz loop bandwidth, the advatage of using an atomic oscillator is negligible.

However, imagine the bandwidth is reduced to on the order of 0.1 Hz. Now, the limits of PSD integration become 0.1 Hz to infinity. And, as shown in Figure 2, this change in integration limits captures the large difference between the crystal and atomic oscillator PSD curves. In this example, an atomic oscillator will have a smaller contribution to the total phase jitter than crystal oscillators.

So, when small bandwidths are desired, atomic oscillators provide a distinct advantage. It is for this reason that they are the focus of this work.

VI. PLL ERROR RESPONSE

The third-order loop filter will not have steady-state tracking error due to acceleration. However, it will have a steady state error due to jerk. In addition, there are transient tracking errors due to step, ramp and acceleration inputs.

The maximum errors (due to dynamic stresses) are difficult to compute. To overcome this issue, a reasonable method is to use the steady-state error due to dynamic stress to approximate the worst case errors. This assumption is reasonable the typical loop filter parameters used in this work (which were discussed in Section II-B) result in very little overshoot for the closed loop system [8]. So, the steady-state error is used as an approximation of the worst case error.

For constant jerk, k_j, to the system in Figure 1, the input may be written as,

$$\varphi_i(t) = \frac{k_j}{6}t^3u(t) \quad \Rightarrow \quad \varphi_i(s) = \frac{k_j}{s^4} \tag{17}$$

where, t is time, $u(t)$ is the unit step function, and s denotes the Laplace domain.

The steady state error due to constant jerk for a third-order PLL is written as,

$$e_{ss} = \frac{k_j}{w_{0,3}^3} = \frac{k_j(0.7845)^3}{B_n^3} \quad [\mathrm{m}] \tag{18}$$

where k_j is in units of $\mathrm{m/s^3}$ [8, p.189]. So, tightening the bandwidth B_n produces a larger steady state error. In addition, the steady state error can be upper-bounded (if the maximum jerk can be computed) as follows,

$$e_{ss,max} = \frac{k_{j,max}(0.4828)}{B_n^3} \quad [\mathrm{m}] \tag{19}$$

$$= \frac{360}{(0.19)}\frac{k_{j,max}(0.4828)}{B_n^3} \quad [\mathrm{degL1}] \tag{20}$$

where $k_{j,max}$ is in units of $\mathrm{m/s^3}$.

The following sections discuss important sources of error and their impact on the PLL. Satellite motion error (Section VII) and nominal ionosphere (Section VIII) are modelled as dynamic stresses. Finally, all contributions to total phase jitter are assembled in Section IX, where the minimum theoretical bandwidth is determined.

VII. SV MOTION

Satellite motion must be tracked with low phase error if we wish to use GPS positioning. SV motion, is a vital/integral part of GPS operation and allows for measurements taken over time to improve static positioning capability.

For our third-order PLL, the jerk due to SV motion is accounted for as a dynamic stress because it cannot be analyzed in a statistical sense. Equation 20 provides the ability to compute an upper bound on the impact of SV motion on the PLL phase jitter. However, the maximum global jerk $k_{j,max}$ due to SV motion must be determined.

Satellite motion causes the user-to-satellite range to vary smoothly other time, so it is not expected that the maximum jerk will be very large (i.e. or a dominant source of jitter at all bandwidths). However, when attempting to tighten bandwidth to the extreme, SV motion cannot be neglected if an accurate theoretical computation of minimum bandwidth is desired. In other words, for very small bandwidths it may become a non-negligible contribution to phase jitter.

To compute jerk due to satellite motion, user-to-satellite range is triple-differentiated with respect to time [7, p. 389]. For illustration purposes, Figure 3 shows the range as a function of time for PRN 4 and 7 (computed using the GPS Standard Positioning Service (SPS) almanac [11]) for a stationary user located at 35N, -150E. After numerically differentiating three times, the resulting jerk profiles are shown in Figure 4. Then, for this example, the maximum absolute jerk value for each PRN can be determined, followed by the maximum overall jerk for any PRN.

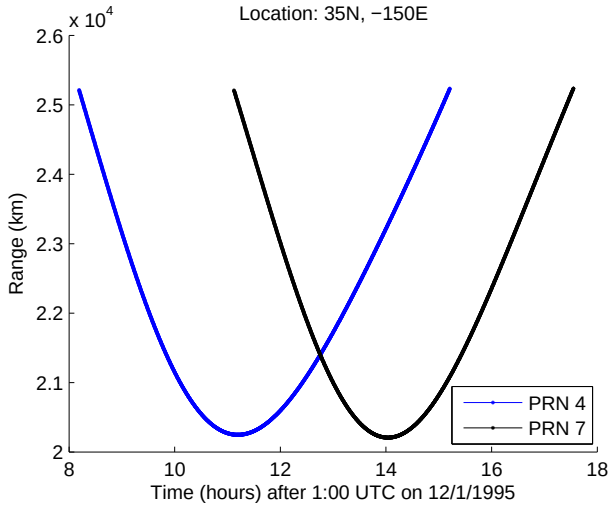

Fig. 3. Example illustrating satellite range as a function of time for PRN 4 and 7

To compute the maximum global jerk, a simulation is conducted using all satellites, and computing range to each satellite over a 24 hour period, for a grid of 1825 locations. Locations from -60N to 60N latitude in 5 degree increments, and 5 degree longitude increments were used. The maximum global satellite motion jerk computed using the almanac is determined to be $k_{j,max} = 2.21 \times 10^{-5}$ m/s^3. Using a recent broadcast ephemeris, the maximum jerk is $k_{j,max} = 2.64 \times 10^{-5}$ m/s^3. The maximum jerk values computed using the almanac and ephemeris are very similar. Since the broadcast ephemeris jerk value is larger, it is used in the remainder of the phase jitter analysis.

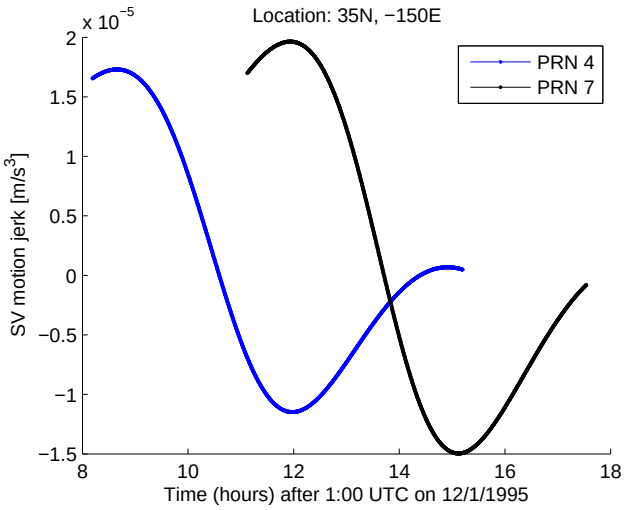

Fig. 4. Example illustrating jerk due to SV motion as a function of time for PRN 4 and 7

Figure 5 shows steady state error due to satellite motion jerk versus loop bandwidth computed using equation 20. The steady state error is given in degrees L1.

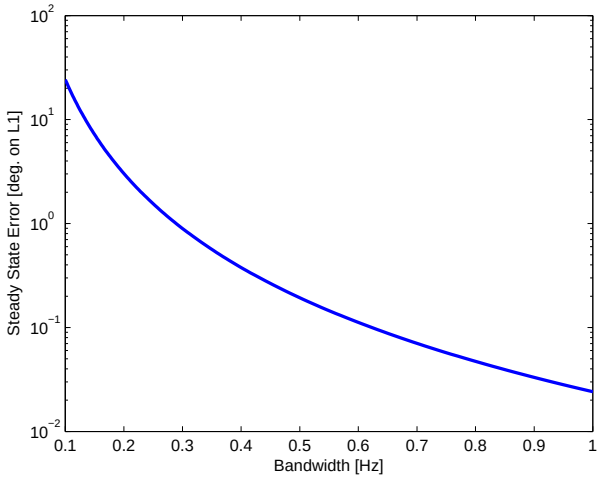

Fig. 5. Steady State error due to max global jerk due to SV motion, in degrees L1

The range of bandwidth in Figure 5 is less than 1 Hz. At a 0.1 Hz bandwidth, the error is roughly 24 degrees L1, which corresponds to about 13mm. It seems that this error alone would exceed the phase jitter threshold set in section III-A. However, dynamic stresses are weakened by a factor of 3 in the phase jitter equation (equation 10). For typical PLL bandwidths, about 25 Hz, the jerk due to satellite motion is not a significant contribution to total phase jitter, which is why some other theoretical analyses, [14], [6], were reasonably accurate without including this error source. Again, since this work seeks the minimum theoretical bandwidth (to reject as much wideband interference as possible), SV motion will

become a significant contribution to phase jitter.

VIII. NOMINAL IONOSPHERE

Another important dynamic stress error is that due to the nominal ionosphere. Nominal ionosphere does not include ionospheric fronts, anomalies or scintillation.

The existing method to model the nominal ionosphere error for a third-order loop, involves using the steady state error equation (approximately worst case) for a first-order loop [7, p.389],

$$\theta_{e,iono} = \frac{2\pi\Delta f_{max}}{4B_n} \text{ [rad]} = \frac{360\Delta f_{max}}{4B_n} \text{ [deg]} \tag{21}$$

where, an upper bound on the frequency shift, Δf_{max}, caused by the ionosphere is 0.085 Hz for a stationary GPS user [7, p. 495]. This model has been implemented in [14], where the result was significant phase jitter due to iono for bandwidths less than 1 Hz.

The conventional model proposed in [7] is believed to be unrealistically conservative because it assumes that the iono would cause an abrupt frequency shift. On a global scale, large spatial gradients may be observed in the total electron content (TEC) in the ionosphere. However, as the user-to-satellite line of sight (LOS) changes smoothly with time, the observed changes in TEC should also vary continuously with time. This would imply a smoothly changing delay on L1, and therefore a lower jerk error than predicted by the previous model.

In this work, the international reference ionosphere (IRI) 2012 model is used to determine the maximum jerk due to the nominal ionosphere [2]. Then, the dynamic stress equation 20 can be used to compute the iono contribution to phase jitter. So, this simulation parallels the one done for the satellite motion problem.

To begin, for a given user location and time of day, the IRI model is used to compute electron densities at points within the ionosphere along the user-satellite LOS. This is illustrated in Figure 6, with discretized points in the ionosphere, between 65 km and 2000 km altitude.

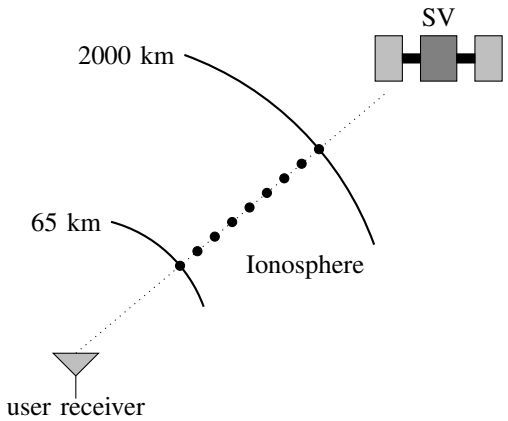

Fig. 6. Discretized points in ionosphere along LOS, at which electron densities are computed

The electron density, N_e, is integrated along the LOS to approximate the slant TEC content,

$$TEC = \sum N_e \Delta l \tag{22}$$

where Δl is the distance between discretized points in the ionosphere. Finally, the iono delay on L1 (in meters) can be determined as [12],

$$I_\rho = \frac{40.3\ TEC}{f_{L1}^2} \tag{23}$$

This was for a single user location and time. Propagating SV geometry forward in time, the iono delay as a fuction of time can be determined. Then, it is a matter of triple-differentiating w.r.t. time, and determining the maximum value of jerk. Again, this procedure is analogous to what was done for SV motion jerk. Figure 7 depicts a sample computation of the delay on L1 frequency caused by the ionosphere. Figure 8 is the jerk profile resulting from triple-differentiating the curve in Figure 7 with respect to time.

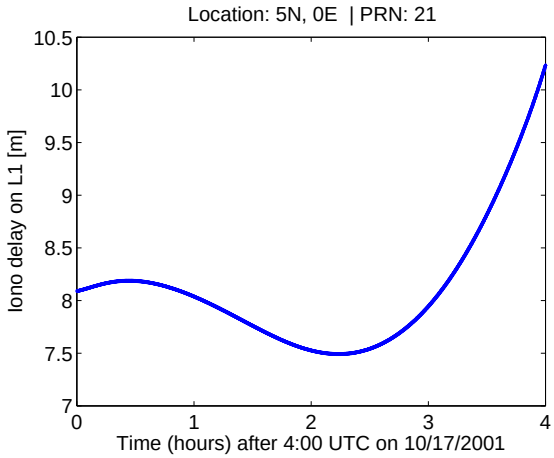

Fig. 7. Example illustrating ionospheric delay on L1

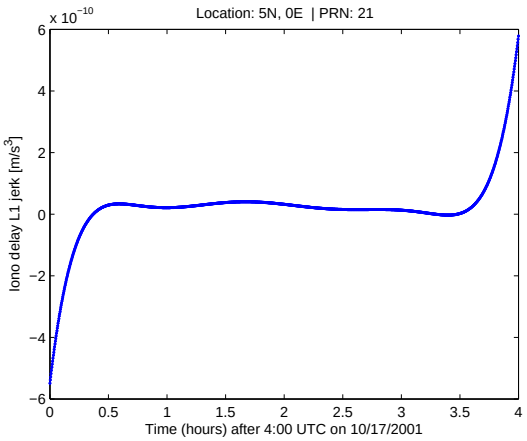

Fig. 8. Example illustrating jerk due to nominal ionosphere

Ideally, to compute the maximum global jerk due to nominal ionosphere using the IRI2012 model, another 24 hour

simulation using a grid of 1825 locations would be used. However, this was not feasible due to computational burdens. Instead, a single worst-case (geomagnatic) equatorial location, 5 degrees North, 0 degrees East, was used. In addition the year 2001 is simulated using the IRI model, which corresponds to solar maximum. And, to maximize the probability of capturing large dynamics in nominal TEC content, the hours 4:00-8:00 UTC, are simulated for all 24 satellites in the nominal GPS constellation. This time period places the early morning TEC gradient directly overhead of the equatorial location.

The maximum jerk due to the ionosphere observed through this simulation is $k_{j,max} = 1.15 \times 10^{-7}$ m/s^3. So, based on the IRI model, the jerk due to nominal ionospheric is less than that due to SV motion.

IX. MINIMUM THEORETICAL BANDWIDTH RESULTS

To reject the maximum level of wideband interference (i.e. white noise) the goal in this work is to determine the minimum allowable PLL bandwidth that satisfies a phase jitter threshold of 10 degrees, set in Section III-A.

Figure 9 shows the contributions to total phase jitter plotted separately. Dynamic stresses are divided by a factor of 3, according to equation 10. The thermal noise curve is plotted for $C/N_0 = 30$ dB-Hz and $T_{CO} = 1$ ms. This figure illustrates the trade-off between noise performance and dynamic performance. The contribution to total phase jitter due to thermal noise decreases as PLL bandwidth is decreased. However, the contributions due to SV and receiver clock noise as well as dynamic stresses (due to SV motion and nominal ionosphere) increase as the bandwidth is decreased.

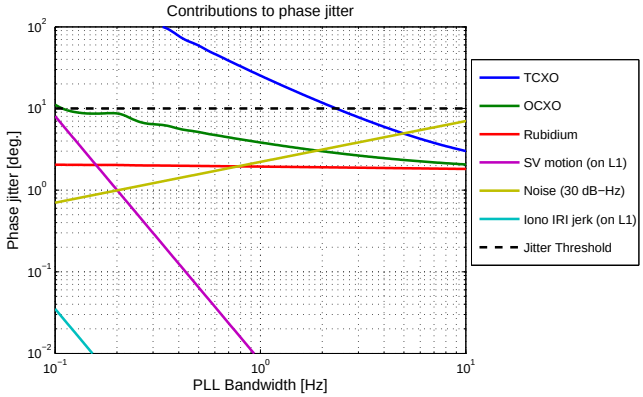

Fig. 9. Contribution to phase jitter

The sources of phase jitter typically used in the design of stationary PLLs include receiver thermal noise, as well as satellite and receiver clock noise [5]. Figure 10 shows the resulting total phase jitter (computed using equation 10) when only these sources are considered. The less conservative rubidium PSD is used to represent the PSD of satellite clocks. TCXO and rubidium receiver clock results (blue and red curves repectively) are plotted for varying carrier-to-noise ratios between 20 and 40 dB-Hz to show how the presence of wideband interference affects the results. As an example, this theory indicates that when using a rubidium oscillator, bandwidths less than 0.4 Hz, and down to at least 0.1 Hz, are achievable for a 20 dB-Hz carrier-to-noise ratio.

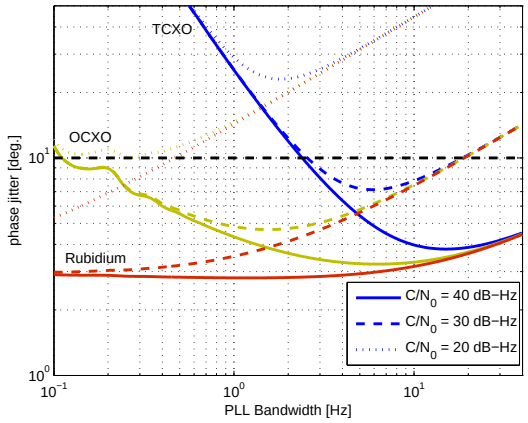

Fig. 10. Total phase jitter with nominal contributions only

Now, putting all the contributions in Figure 9 together, including satellite motion and nominal ionosphere, and using the total phase jitter rule, equation 10, yields Figure 11. Both TCXO and rubidium receiver oscillator results are plotted (again, blue and red curves repectively), including the effects of dynamic stresses due to SV motion and nominal ionosphere. Multiple phase jitter curves are shown, with carrier-to-noise ratios varying between 15 and 40 dB-Hz, to show the impact of wideband interference.

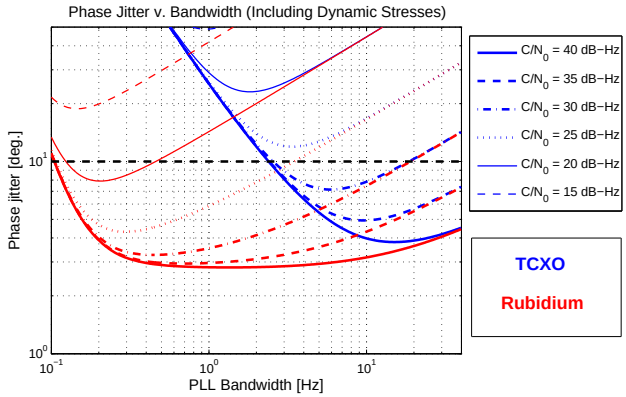

Fig. 11. Total phase jitter

Comparing Figures 11 and 10, the TCXO results appear very similar. However, there is a noticeable increase in total phase jitter for rubidium results when PLL bandwidth is tightened below about 0.2 Hz. For example, Figure 11 shows that for a 20 dB-Hz carrier-to-noise ratio, the PLL bandwidth must be roughly between 0.15-0.4 Hz to satisfy the phase jitter metric. Comparing this result to that of Figure 10, it is clear that the addition of dynamics stresses due to satellite

motion and nominal ionosphere are responsible for the lower bandwidth limitation.

The theoretically predicted system performance from Figure 11 shows reliable tracking can be achieved with signal C/No level of 25 dB-Hz using a rubidium oscillator and PLL bandwidth of 0.25 Hz. This result is in the absence of ionospheric scintillation.

X. EXPERIMENTAL VALIDATION AND RESULTS

Experimental results presented in this section are used to validate the theoretical analysis. The experiments are performed using an RF signal generator (Spectracom GSG-6) to directly simulate a GPS signal with wideband interference, which is realized as a deteriorated carrier-to-noise ratio. The signal generator also reproduces the effects of satellite motion and ionospheric dynamics. The simulated signal enters into a GPS RF front-end kit, which utilizes an external clock input from a commercially available rubidium clock. A Universal Software Radio Peripheral (USRP) N200, with a DBSRX2 daughterboard, produced by Ettus Research is used as the receiver front-end, which saves complex IQ data sample for post-processing. The rubidium oscillator used in this work is a 10MHz Spectratime LPFRS-01/AV1.

The saved data is post-processed in Matlab using a software-defined receiver (SDR) [3]. A second-order unaided delay-lock loop (DLL) with 2 Hz bandwidth is used throughout this work. Note that the phase error, ϕ, as defined in Figure 1 cannot be measured directly. Only the tracking error, ϵ, is available. There is an existing method, derived in [14], to estimate the variance of phase jitter from the variance of tracking error. This method is discussed in section XI.

It is possible to determine whether the receiver PLL is tracking properly by looking at the tracking error. So, to begin, tracking error results are discussed. Then, in section XI, the relationship between tracking error and the phase jitter theory is analyzed.

A. Effect of receiver clock quality

To emphasize the advantage of using atomic oscillators for receivers, we first look at tracking error at a nominal carrier-to-noise ratio of, $C/N_0 = 45$ dB-Hz (no interference present). The tracking error over time is output from the software-defined receiver (SDR). The 2σ tracking error is computed for an example PRN (i.e. receiver channel) and plotted for various PLL bandwidths in Figure 12, for both TCXO (blue curve) and rubidium (red curve) receiver oscillators.

Even under a nominal carrier-to-noise ratio, the TCXO built into the USRP N200 does not allow bandwidths to be tightened below approximately 10 Hz, at which point the 2σ tracking noise grows rapidly. Using a rubidium (LPFRS-01) oscillator allows the PLL bandwidth to be tightened to 0.15 Hz without large increases in tracking noise. So, rubidium atomic clock results are shown in the remainder of the paper.

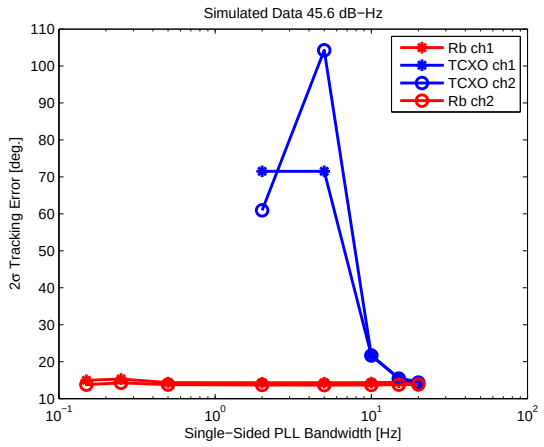

Fig. 12. Tracking error versus bandwidth for nominal C/N_0

B. Tracking Error

A wideband interference scenario can be simulated as additional noise (or weaker signal). This is accomplished by reducing the output power of the Spectracom signal generator. This is in contrast to prior work [5], which simulated interference in Matlab by adding numerically generated noise to the intermediate frequency data samples from the receiver front-end. A rubidium oscillator is used as a reference for the receiver front-end, as well as for the signal generator.

Figure 13 shows the tracking error plotted over time for two example PRNs, when a rubidium receiver oscillator and coherent average time $T_{CO} = 1$ ms are used. Tracking is initiated at a nominal 45 dB-Hz carrier-to-noise ratio because the focus of this work is on the PLL ability to track in the presence of wideband interference. Acquisition under interference conditions is a difficult problem, and not attempted in the present work. So, after the PLL has been locked onto the signal for some time, the carrier-to-noise ratio is rapidly decreased to 25 dB-Hz to simulate the abrupt onset of wideband interference.

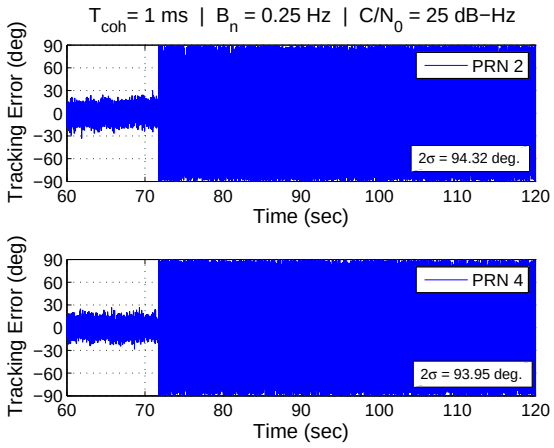

Fig. 13. Tracking error versus time for $T_{CO} = 1$ ms

In Figure 13, the presence of interference causes the peak-to-peak tracking error to increase from less than 30 degrees, to at least 90 degrees. The 2σ tracking error is over 90 degrees. Note that when the tracking error reaches 90 degrees the PLL will cycle slip. Therefore, this is not a good example of robust tracking in the presence of interference. In this example the PLL is constantly cycle-slipping once interference is introduced.

So, these simulation results show that the PLL is losing lock earlier than predicted by the total phase jitter theory. The PLL linear model is based on the assumption that both tracking error and phase error are small. This assuption is used to generate the loop transfer function used in that analysis. However, in this example, the tracking error is clearly not small. So the validity of the linear model in this case is questionable.

To improve the tracking results, and ensure the validity of the linear PLL model, the tracking error should be reduced. To do so, the coherent average time is increased from 1 ms to 20 ms. Figure 14 shows the same tracking error over time results as Figure 13, but for $T_{CO} = 20$ ms. This additional averaging reduces the noise and allows the receiver to track.

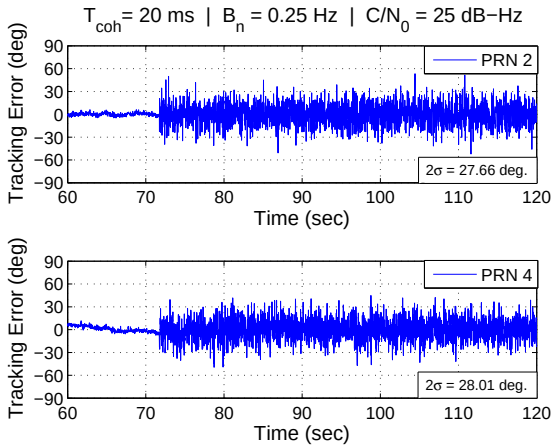

Fig. 14. Tracking error versus time for $T_{CO} = 20$ ms

In this case, the 2σ tracking noise is less than 30 degrees, which is indicative of continuous carrier phase tracking.

But, why does the PLL lose lock earlier than predicted by the total phase jitter metric? This raises question as to whether the phase jitter metric is conservative at all.

XI. DISCUSSION ON TRACKING ERROR AND PHASE JITTER

A procedure is developed in [14] to estimate the variance of total phase jitter from the variance of tracking error. Figure 15 shows the estimated phase jitter from experimental results plotted over the theoretical phase jitter curves.

Both the nominal 45 dB-Hz carrier-to-noise ratio as well as the 25 dB-Hz interference scenario are shown. Two concerns are raised by these results. The first is that, for both cases,

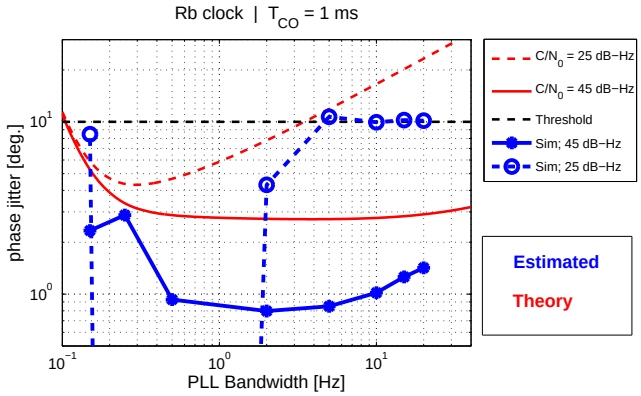

Fig. 15. Comparison between theoretical and estimated phase jitter

the experimentally estimated phase jitter does not match well with the theoretical computation. However, the more important concern is that the estimated jitter results for $C/N_0 = 25$ dB-Hz are below the threshold for PLL bandwidths of 2 Hz and less. This would indicate that the loop is operating in its linear region. However, we already know from Figure 13 that the tracking error is very large for this case. And, in fact, the PLL is not reliably tracking carrier phase.

The phase jitter metric is a useful tool for designing phase-lock loops. It is a necessary condition for reliable tracking. Nevertheless, it is not a sufficient metric, and should be supplemented with tracking error, and/or bit error rate (BER) analysis.

XII. CONCLUSION

In this work, the high stability of atomic clocks (relative to crystal oscillators) is leveraged to significantly reduce the bandwidth of the receiver phase lock loop (PLL), thereby reducing the impact of wideband interference. The main contribution of this paper is a rigorous theoretical computation and experimental validation of the minimum achievable PLL bandwidth, considering all relevant contributions to phase jitter including, thermal noise, satellite and receiver clock noise, nominal ionosphere, and satellite motion. It has been theoretically shown that typically overlooked contributions due to nominal ionosphere and satellite motion become significant at PLL bandwidths below 1 Hz, which are otherwise feasible with atomic clock aiding. The maximum global jerk due to satellite motion has been quantified using recently broadcast ephemeris. Also, the International Reference Ionosphere (IRI) 2012 model has been used to estimate the worst-case jerk due to the nominal ionosphere. These jerk results enable an overbound on the dynamic stresses experienced by a stationary receiver to be quantified.

Experimental results show that for a stationary reference receiver using a rubidium oscillator, the phase-lock loop is able to continuously track carrier phase at a carrier-to-noise ratio of 25 dB-Hz using a 0.25 Hz loop bandwidth and 20 ms

coherent average time. This is 7 dB lower than the 32 dB-Hz standard for GBAS ground stations [4].

Future work includes testing other high quality oscillators, as well as deriving a more accurate method to estimate phase jitter from tracking error. The intent of this study is to gain insight into PLL operation, and the advantages/disadvantages of using the phase jitter metric. The advantages of using the tracking error as a more direct metric of continuity of phase lock will also be investigated.

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References

[1] Gnss jamming in the name of privacy: Potential threat to gps aviation, March/April 2012.

[2] Bilitza, D., et. al. The International Reference Ionosphere 2012 - a model of internatinoal collaboration. *Space Weather and Space Climate*, 4(A07), February 2014.

[3] Borre, K., et. al. *A Software-Defined GPS and Glonass Receiver*. Birkhauser, 2006.

[4] Brenner, M. Simulation of swept fm interference and its impact on an aviation receiver. In *Proceedings of the 26th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2013)*, pages 1359–1370, Nashville, TN, September 2013.

[5] Chan, F.-C., Joerger, M., Khanafseh, S., Pervan, B., Jakubov, O. Performance analysis and experimental validation of broadband interference mitigation using an atomic clock-aided gps receiver. In *Proceedings of the 26th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2013)*, pages 1371–1379, Nashville, TN, September 2013.

[6] Demoz, G.E., et. al. Sensitivity and performance analysis of doppler-aided gps carrier-tracking loops. *Navigation*, 52(2):49–60, 2005.

[7] A. Van Dierendonck. *Global Positioning System: Theory and Applications*. AIAA, Washington, DC, 1996.

[8] Kaplan, E.D., and Hegarty, C. J. *Understanding GPS: Principles and Applications*. Artech House, 2 edition, 2006.

[9] Kraus, T., Bauernfeind, R., and Eissfeller, B. Survey of In-Car Jammers - Analysis and Modeling of the RF Signals and IF Samples (Suitable for Active Signal Cancelation). In *Proceedings of the 24th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2011)*, pages 430–435, Portland, OR, September 2011.

[10] Mitch, R.H., et. al. Signal Characteristics of Civil GPS Jammers. In *Proceedings of the 24th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2011)*, pages 1907–1919, Portland, OR, September 2011.

[11] Department of Defense. Global positioning system standard positioning service performance standard, September 2008. Available online at http://www.gps.gov/technical/ps/2008-SPS-performance-standard.pdf.

[12] P. Misra and P. Enge. *Global Positioning System: Signals, Measurements and Performance*. Ganga-Jamuna Press, Lincoln, MA, 2006.

[13] R. S. Conker, M. Bakry El-Arini, C. J. Hegarty, and T. Hsiao. Modeling the effects of ionospheric scintillation on gps/satellite-based augmentation system availability. *Radio Science*, 38(1), 2003.

[14] Razavi, A., Demoz, G.E., and Akos, D.M. Carrier loop architectures for tracking weak gps signals. *IEEE Transactions on Aerospace and Electronic Systems*, 44(2):697–710, 2008.