

Quantifying Phase Lock Loop Robustness Through Interference using the Phase Discriminator Output

Wengxiang Zhao
Department of MMAE
Illinois Institute of Technology
Chicago, United States
wzhao42@hawk.iit.edu

Stefan Stevanovic
Department of MMAE
Illinois Institute of Technology
Chicago, United States
sstevano@hawk.iit.edu

Boris Pervan
Department of MMAE
Illinois Institute of Technology
Chicago, United States
pervan@iit.edu

Abstract—In this paper, we develop a PLL performance measure that allows phase lock loop design parameters to be determined given a mean time to cycle slip requirement. This concept is directly applicable to both stationary and moving GPS receivers subject to wideband radio frequency interference.

The PLL performance metric developed in [1] is improved to rule-out inadequate PLL designs and allow time-consuming experimental validation to be reserved for designs that are more likely to be successful. This is accomplished by using direct non-linear PLL simulation to quantify the relationship between the discriminator output standard deviation and the mean time to cycle slip. This relationship can then be used to determine a suitable threshold for the DO standard deviation given a mean time to cycle slip requirement, which will depend on the particular application of interest. Then the phase lock loop parameters that are necessary to achieve this mean time to cycle slip can be determined analytically.

Additional simulation results show that DO standard deviations less than 52 degrees correspond to more favorable DO distributions, and this translates to longer mean time to cycle slip. In addition, our results further validate the DO metric by showing that increasing coherent averaging time is the only way to obtain substantial increases in mean time to cycle slip under interference conditions.

Index Terms—GPS receiver, Phase Lock Loop, Wideband Interference, Discriminator Output

I. INTRODUCTION

In this work, we develop a performance measure for GPS receiver phase lock loop (PLL) that are subjected to wideband radio frequency interference (RFI). This technique allows PLL design parameters to be determined given requirements for mean time to cycle slip (MTCS) and wideband interference sensitivity. This concept is directly applicable to both stationary GPS reference receivers as well as moving receivers.

The example application used to illustrate the new performance criterion is GBAS reference station receivers subjected to broadband interference — for example, from nearby use of personal privacy devices (PPDs). Prior work has shown that PPDs most commonly emit broadband interference, and GBAS ground based reference receivers have experienced tracking discontinuities as a result [2]. These events can cause navigation service interruptions to aircraft on final approach. To ensure continuity of the navigation service GBAS reference stations must be able to track GPS signals in the presence of wideband interference.

It is known that in order to track through increased wide-band noise levels, the PLL coherent averaging time must be increased from the typical 1 ms duration. However, there exists a trade-off between noise rejection and dynamic performance. In this work, we use a low phase-noise receiver reference oscillator to allow the PLL bandwidth to be tightened and averaging time extended, ensuring uninterrupted tracking of carrier phase.

A popular metric used to predict the lock performance of a PLL under noisy conditions is the total *phase jitter* metric [3], [4], [5], [6]. A major advantage of this metric over more rigorous/accurate performance evaluation tools, such as computing the mean time to cycle slip (MTCS) using non-linear theory, is in its analytical simplicity. The jitter metric is based on a linear PLL model, and is able to account for the additional effects of oscillator phase-noise and dynamics. Additional considerations such as oscillator phase-noise and dynamic effects are not currently within the capability of the non-linear theory.

However, the phase jitter metric has some major drawbacks. According to this metric, reducing PLL bandwidth is the most effective countermeasure against wideband interference. Results from prior research, [3] [4] [5] [6], relying on this metric, consistently state that in experiments, loss of lock occurs at C/N_0 values that are higher than predicted by the phase jitter metric.

In our prior work [1], we proposed that the standard deviation of the phase discriminator output (DO) be used as a PLL performance design metric and expound the advantages of this metric over the popular phase jitter metric using theory, numerical simulation, and experimental results. Our results have shown that the PLL DO standard deviation is more indicative of phase-lock performance than the popular phase jitter metric. And, a PLL performance metric was created by comparing the DO standard deviation to a threshold derived from the DO distribution. The distribution of the DO was shown to transition from Gaussian-like to a uniform distribution depending on the carrier-to-noise ratio and PLL averaging time. In [1] we placed a threshold of 52 degrees on the DO standard deviation (corresponding to a uniform DO distribution), which created a feasibility test. This feasibility test was shown to reduce the need for time-

consuming simulations and experimental validation. Any PLL designs resulting in a DO standard deviation larger than 52 degrees are immediately known to be inadequate and unable to robustly track carrier phase.

In this paper, the PLL performance metric developed in [1] is improved to rule-out additional inadequate PLL designs. This is accomplished by using direct non-linear PLL simulation to quantify the relationship between the DO standard deviation and the mean time to cycle slip (MTCS). This relationship can then be used to determine a suitable threshold for the DO metric given a MTCS requirement, which will depend on the particular application of interest.

Simulation results show that DO standard deviations less than 52 degrees correspond to more favorable DO distributions, and that this translates to longer MTCS. In addition, our results further validate the DO metric by showing that increasing coherent averaging time is the only way to obtain substantial increases in MTCS under interference conditions. In contrast, the phase jitter metric predicts that that tightening PLL bandwidth is sufficient.

Section II in this paper describes PLL operation and the augmented PLL linear model corresponding with the DO metric. In section III, the DO metric is introduced, and an example PLL is designed using this metric. Finally, section IV discusses the MTCS results from direct non-linear PLL simulation.

II. PLL OPERATION

The phase lock loop (PLL) is a feedback control system that creates a replica carrier signal and attempts to keep its frequency and phase aligned with that of the incoming carrier signal. This work focuses specifically on the PLL because it is most susceptible to wideband interference, and will lose lock before the delay-lock loop (DLL) does [4]. Figure 1 shows the PLL block diagram. The input to the PLL is the intermediate frequency (IF) signal $s(t)$, which may be written for a single satellite as,

$$s(t) = \sqrt{2CD}x(t) \cos(\omega_{IF}t + \psi(t)) + n_s(t) \quad (1)$$

where C is the signal power, D is the navigation data message, x is the code, ω_{IF} is the intermediate frequency (in rad/s), $n_s(t)$ is additive white Gaussian noise (AWGN), and $\psi(t)$ is the phase process which includes all Doppler effects due to user and satellite motion, as well as both receiver and satellite clock instabilities. The receiver clock instability is a consequence of the down-conversion in the receiver's front-end. Wideband RFI is modeled as AWGN.

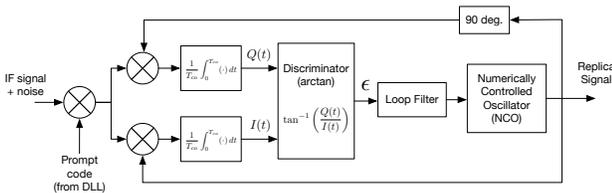


Fig. 1. Phase lock loop block diagram

The input signal is first multiplied by the code replica obtained from the receiver's delay lock loop (DLL). This process is called code wipe-off because if the replica code is aligned perfectly with the incoming, the code will be removed from the signal. In this work, perfect code alignment is assumed, which allows the signal, after mixing with prompt code, to be written as,

$$y(t) = \sqrt{2CD} \cos(\omega_{IF}t + \psi(t)) + n(t) \quad (2)$$

The signal $y(t)$ is then multiplied by in-phase and quadrature replica signals, x_I and x_Q respectively, generated by the numerically controlled oscillator (NCO),

$$x_I(t) = \sqrt{2}K \cos(\omega_{IF}t + \hat{\psi}(t)) \quad (3)$$

$$x_Q(t) = -\sqrt{2}K \sin(\omega_{IF}t + \hat{\psi}(t)) \quad (4)$$

where $\hat{\psi}(t)$ is the replica phase process. This mixes the signal down to baseband (carrier wipe-off). Then there is a coherent averaging (i.e. integrate and dump) operation followed by the discriminator, which is sometimes called a phase detector because it estimates the phase error between input and replica signals. The loop filter is a compensator designed to achieve desired system response, and it designates the 'order' of the phase lock loop [7]. The loop filter output is fed to the numerically controlled oscillator (NCO) which generates the replica carrier signals, and closes the loop. Additional detailed information on the complete GPS signal processing technique (from signal capture at the antenna through pseudorange computation) is available in [7] [8] [9].

The receiver clock is a reference input to the NCO. Therefore, the receiver clock phase-noise can be modeled as a disturbance on the NCO output. However, in this work, the PLL is implemented in a software defined receiver (SDR), and there is no additional phase-noise contribution from the NCO. The effect of both satellite and receiver oscillator phase noise will enter the PLL through the input signal (due to mixing in the receiver front-end). In addition, our PLL uses the common two-quadrant arctangent discriminator and a third-order loop filter (more on the loop filter in the following).

A. Augmented PLL Linear Model

The "augmented" linear model shown in Figure 2 was derived in [1], where the transfer functions $C(s)$, $F(s)$, and $G(s)$ correspond to the coherent integration, loop filter and NCO respectively. It differs from the conventional PLL linear model in that it considers the effect of coherent averaging (modeled as a moving average). In addition, this figure illustrates the definition of phase error, ϕ , and discriminator output, ϵ , which is an estimate of the true phase error, ϕ . The popular total phase jitter performance metric computes the standard deviation of phase error, ϕ . In [1], we proposed an improved performance metric based on the discriminator output. The phase error and discriminator output are related by,

$$\epsilon(t) = \langle \phi(t) + n'_Q(t) \rangle \quad (5)$$

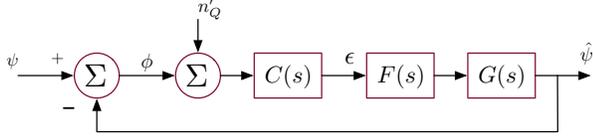


Fig. 2. Augmented PLL linear model

where brackets are used to denote the coherent averaging operation.

In Figure 2, the AWGN input is represented by n'_Q , and since our PLL is implemented in software, there is no phase-noise contribution from the NCO. The phase-noise of both the receiver and satellite clocks will only enter the PLL through the input phase process, ψ , due to mixing in the receiver front-end. When working with traditional receivers, the added phase-noise contribution from the NCO can easily be included. Its absence in our particular PLL implementation does not affect the analysis techniques or conclusions reached using this linear model.

It is worth noting that the only difference between this augmented linear model and the conventional linear model [10] is the additional effect of coherent averaging, $C(s)$. It is included to obtain a more accurate transfer function from AWGN input to discriminator output.

The PLL performance and design metric this work focuses on is based on the discriminator output [1]. The variance of the discriminator output, σ_ϵ^2 , may be expressed using the Wiener-Khinchin theorem. To do so, we need the transfer function from the noise and phase inputs to the discriminator output, which we will call the “discriminator output transfer function”.

Using $C(s)$ to denote the transfer function for the coherent averaging, the discriminator output transfer function, H_D , is,

$$H_D(s) = \frac{C(s)}{1 + C(s)F(s)G(s)} \quad (6)$$

This transfer function describes the following input-error relation,

$$\epsilon(s) = H_D(s) (n'_Q(s) + \psi(s)) \quad (7)$$

Then, the variance of the *discriminator output*, ϵ , can be computed as,

$$\sigma_\epsilon^2 = \int_0^\infty |H_D(j2\pi f)|^2 (S_{n_i}(f) + S_{clk}(f)) df \quad (8)$$

where $S_{n_i}(f)$ is the single-sided PSD of the noise input, n'_Q , and $S_{clk}(f)$ is the single-sided PSD of clock phase noise.

It can be shown that the relationship between the input noise PSD and carrier to noise ratio is,

$$S_{n_i}(f) = \frac{1}{(C/N_0)} \quad (9)$$

when $C = 1$ and $K = 1$; These values are chosen for convenience in our simulations. The modeling of oscillator phase noise PSDs is discussed in [1].

To evaluate $H_D(s)$, we must define $C(s)$, $F(s)$, and $G(s)$. The integrate and dump operation (i.e. coherent averaging) will be approximated using a moving average. The transfer function for a moving average can be expressed as,

$$C(j\omega) = \frac{T}{T_{co}} \frac{1 - e^{-j\omega T_{co}}}{1 - e^{-j\omega T}} \quad (10)$$

where, T is the sampling period and T_{co} is the coherent integration time [1]. The loop filter (3rd-order) and NCO transfer functions are given by,

$$F_3(j\omega) = \frac{b_3 w_{0,3}(j\omega)^2 + a_3 w_{0,3}^2(j\omega) + w_{0,3}^3}{(j\omega)^2} \quad (11)$$

$$G(j\omega) = \frac{1}{j\omega} \quad (12)$$

A third-order loop filter is considered because of its superior ability to handle dynamics, and additional design freedom compared to a second-order loop [3]. It has zero steady-state error to acceleration stress. However, there will be a steady-state phase error for jerk stresses [7].

The third-order loop filter coefficients a_3 , b_3 , and $w_{0,3}$ are chosen based on the design requirements. One important design consideration is the equivalent noise bandwidth, often simply referred to as the bandwidth. The loop filter coefficients used in this work are, $a_3 = 1.1$, $b_3 = 2.4$, and $w_{0,3} = 0.7845B_n$, where, a_3 and b_3 are chosen to be the typical third-order loop filter coefficients specified in [7].

III. DISCRIMINATOR OUTPUT DISTRIBUTION AND VARIANCE-BASED PERFORMANCE METRIC

In this section, the concept of the PLL design metric based on the variance of the DO, σ_ϵ , is introduced. This metric was proposed in our prior work [1], and shown to be more indicative of phase-lock than the popular “phase jitter” metric. To illustrate how the DO metric may be used, an example PLL is designed to maintain continuous phase-lock during interference events. This design example will motivate the need to reduce the DO metric threshold below 52 degrees, to yield a more favorable DO distribution. Quantifying the threshold is discussed in section IV.

In the absence of dynamic stresses, the discriminator output performance metric may be written as,

$$\sigma_\epsilon \leq R \quad (13)$$

where σ_ϵ is the DO standard deviation computed using equation 8, and R is the threshold. In our prior work [1], a threshold of 52 degrees is used as a feasibility limit.

As σ_ϵ increases (because of increased noise level), the discriminator output distribution approaches a uniform distribution over the discriminator’s pull-in region, saturating at a standard deviation of 52 degrees (corresponding to that of a uniform distribution) [1]. At this point, the discriminator is said to be in a “saturated” condition. Therefore, a threshold R of 52 degrees serves as a feasibility limit for maintaining carrier phase tracking. If the tracking error is uniformly distributed, the loop filter will not be able to provide appropriate

steering input to the NCO. Therefore, the mean-time to cycle slip (MTCS) will likely be extremely short and the PLL is not able to maintain tracking lock at all. For this reason, the threshold value R should be lowered in order to reduce the maximum tolerable discriminator output standard deviation. This will yield a PLL design with a more significant MTCS, by ensuring that the discriminator output distribution does not become uniform. The focus of this work is on quantifying the threshold R as a function of MTCS.

The following section illustrates the concept of discriminator saturation for the case with additive white Gaussian noise (AWGN) only.

A. Feasibility study for the AWGN only case

Figure 3a shows the standard deviation of discriminator output, σ_ϵ , versus PLL bandwidth for $T_{co} = 1$ ms and varying C/N_0 . We know that σ_ϵ must remain below the discriminator's saturation level of 52 degrees for the arctangent discriminator. The saturation threshold represents the level at which the tracking error becomes uniformly distributed over the discriminator's pull-in region.

As the carrier-to-noise ratio is decreased from 45 dB-Hz to 30 dB-Hz, the discriminator output standard deviation increases. In addition, note that the PLL bandwidth does not affect σ_ϵ . For a 1 ms coherent averaging time, the lowest feasible C/N_0 that can be tracked is around 30 dB-Hz. Since tightening the PLL bandwidth does not impact σ_ϵ , increasing the coherent averaging time is the only option.

Figure 3b shows the same curves, but for $T_{co} = 20$ ms, corresponding to the duration of a navigation data bit. Compare the $C/N_0 = 30$ dB-Hz curves in Figures 3a and 3b. As T_{co} is increased from 1 ms to 20 ms, σ_ϵ drops from around 40 degrees to 10 degrees. Note that when $T_{co} = 20$ ms, σ_ϵ begins to increase with increasing bandwidth. This increase in standard deviation has been noted in prior work [5], and it does not affect our theoretical conclusions since it is not caused by AWGN. It is caused by the PLL bandwidth approaching $\frac{1}{2T_{co}}$, the bandwidth of the coherent averaging, which is leading to loop stability issues. The results in Figure 3 clearly show that for a given T_{co} the discriminator output variance, σ_ϵ^2 , is not a function of the PLL bandwidth. But, increasing the coherent average time significantly reduces σ_ϵ^2 . Since only AWGN is considered, this shows the best performance possible, i.e. with a perfect oscillator.

So, for a 20 ms coherent averaging time, the discriminator becomes fully saturated at $C/N_0 = 15$ dB-Hz. According to the discriminator output performance metric, to enable the PLL to track at 15 dB-Hz, the averaging time must be increased beyond the length of a navigation data bit.

In the next section we design a PLL capable of continuously tracking the carrier-phase at $C/N_0 = 15$ dB-Hz by increasing the averaging time to 100 ms.

B. PLL design for extended T_{co}

Using the discriminator saturation threshold of 52 degrees on the standard deviation of discriminator output, σ_ϵ , is

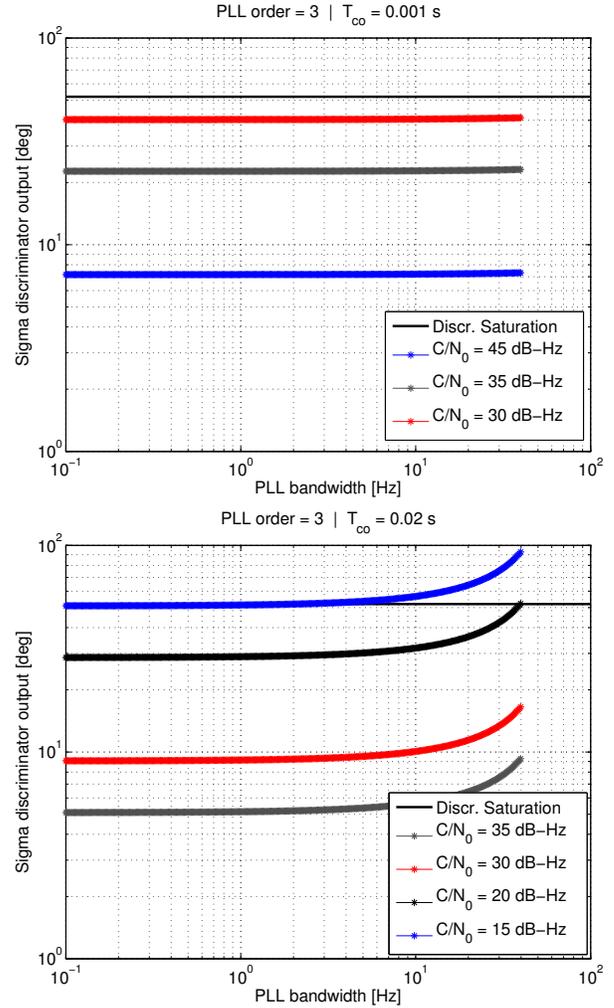


Fig. 3. AWGN only; 1ms and 20ms averaging

adequate for a quick feasibility test. However, in this section, we aim for lower discriminator output variance threshold R in equation 13 to ensure our PLL design yields a favorable discriminator output distribution. Here, in this design example, we are using $\sigma_\epsilon \leq 22.5$ degrees for illustration purposes only. This threshold will be quantified later in section IV.

Figure 4 shows σ_ϵ versus bandwidth for $C/N_0 = 15$ dB-Hz with a proposed $T_{co} = 100$ ms. There are three curves plotted, which correspond to the AWGN only case, as well as when TCXO and OCXO clock models are included. They overlap for bandwidths larger than about 4 Hz. However, at smaller bandwidths clock phase-noise adversely affects σ_ϵ . The discriminator saturation threshold and the 22.5 degree design benchmark are also shown in the figure.

Immediately noticeable in Figure 4 is the large peak in σ_ϵ around 10 Hz bandwidth. This is caused by the same instability described previously when discussing Figure 3b. Feasible design bandwidths are those to the left of the peak.

Based upon these results, we determine that a TCXO is not suitable for this PLL design. The PLL requires a large coherent

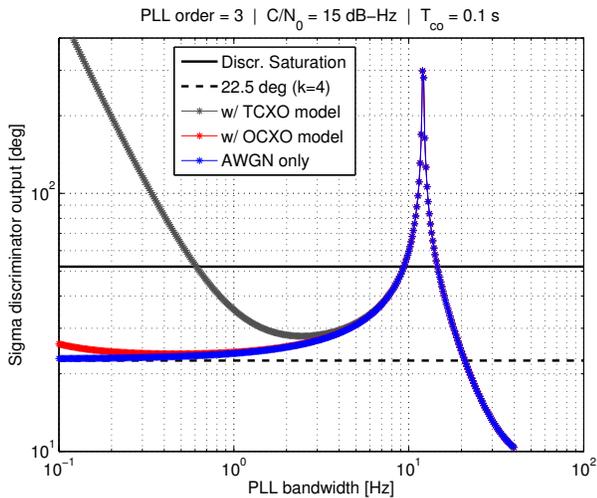


Fig. 4. Standard deviation of discriminator output versus PLL bandwidth

averaging time to handle a $C/N_0 = 15$ dB-Hz, and the PLL bandwidth would need to be reduced to avoid stability issues. However, the phase-noise of the TCXO does not allow for any significant bandwidth reduction. The smallest σ_ϵ for the TCXO curve is about 28 degrees, which does not meet our 22.5 degree design benchmark.

The lower phase-noise of the OCXO does allow the PLL bandwidth to be tightened without adversely affecting σ_ϵ . The OCXO curve only begins to deviate from the AWGN-only case for bandwidths smaller than 0.4 Hz. In addition, $\sigma_\epsilon \approx 23$ degrees, for a 0.4 Hz bandwidth which agrees well with our desired design benchmark of 22.5 degrees.

Therefore, according to the theory, a PLL with a 100 ms averaging time and 0.4 Hz bandwidth should be sufficient to enable the PLL to maintain continuous phase-lock at $C/N_0 = 15$ dB-Hz.

C. Discriminator Output Distribution

To investigate the role of the discriminator in carrier tracking, the probability distribution of the tracking error is determined analytically and examined for varying coherent averaging time. In this exercise, we assume the phase error ϕ is constant in time, and that navigation data bits are known. Therefore, only $n'_I(t)$ and $n'_Q(t)$ are random variables. The discriminator output may be expressed as,

$$\epsilon(t) = \tan^{-1} \left(\frac{\sin \phi(t) + \langle n'_Q(t) \rangle}{\cos \phi(t) + \langle n'_I(t) \rangle} \right) \quad (14)$$

with the coherent averaging only affecting the additive noise terms. The argument of the arctangent becomes a ratio of two Gaussian random variables with non-zero means. The resulting distribution of the discriminator output is derived in figure 5

Figure 5 shows the probability distribution of the discriminator output, ϵ , for a 15 dB-Hz carrier-to-noise ratio and (an example) true phase error, ϕ , of 10 degrees. The distributions

corresponding to three different averaging times are plotted. The figure legend includes the error with respect to the true phase error of 10 degrees (using the expected value to estimate the phase error), as well as the standard deviation of the distribution.

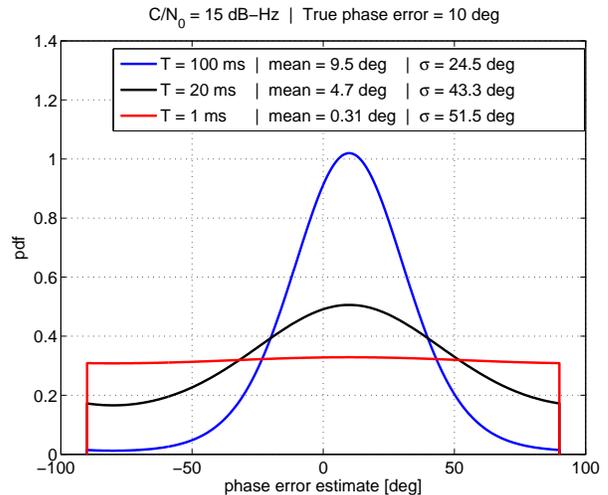


Fig. 5. DO distribution; data bits assumed known

For the example PLL design using 100 ms averaging time, Figure 5 shows that the discriminator output has a very Gaussian-Like distribution. The true phase error can be accurately estimated from this distribution using the expected value. For shorter averaging times, approaching 1 ms, the DO distribution approaches a uniform distribution. This makes it increasingly difficult for the loop filter (modeled by the expected value operator in this example) to obtain a reasonable estimate of the true phase error.

Notice that as the averaging time is decreased and the discriminator output distribution becomes more uniform, the mean of the distribution approaches zero which means a bigger bias. The bias, not the variance, of the distribution is the leading cause of cycle slips. However the DO metric works well for averaging times less than the length of a navigation data bit because it imposes a limit on the variance of the distribution, and also the bias. In our prior work [11], the effect of extended averaging on the discriminator output distribution is studied in detail. And, we have shown that when extending coherent averaging time method using the non-coherent method from [12], imposing a limit on the DO standard deviation still imposes a limit in the DO bias. So, the DO metric can be used to design PLLs with averaging times longer than one navigation data bit.

IV. QUANTIFYING MEAN TIME TO CYCLE SLIP USING TRACKING SIMULATION

In this section, direct non-linear PLL simulation is used to quantify PLL performance in wideband interference using the MTCS. Estimating the MTCS is the most straightforward metric used to quantify interference robustness of a PLL. The

effects of clock phase-noise, signal dynamics, and navigation data bits are not simulated in order to isolate the effects of AWGN. These effects will be part of future work.

A. Effect of PLL parameters on MTCS

Figure 6 shows the MTCS versus averaging time for a 12 dB-Hz carrier-to-noise ratio. Two curves are plotted, which correspond to bandwidths of 15 Hz and 0.4 Hz. The 15 Hz bandwidth corresponds to a nominal bandwidth, and 0.4 Hz is the tightest bandwidth that can be achieved using a low phase-noise oscillator [1].

For each simulation point shown in the figure, 100 trials are conducted and mean value of MTCS is computed. In addition, 1σ error bars are shown. The MTCS results for all PLL bandwidths between 0.4 Hz and 15 Hz will lie in the area between the two curves in Figure 6. When the coherent averaging time T_{co} approaches $\frac{1}{2B_n}$, the PLL will encounter a stability issue [5] [1]. Therefore, increasing T_{co} also requires the bandwidth to be tightened. This relationship would form a bound on the right-hand side of Figure 6.

Figure 6 can be used to explain the difference between the phase jitter metric and the DO metric. According to the jitter metric decreasing PLL bandwidth improves tracking performance in wideband interference. First consider a typical 1 ms averaging time and 15 Hz bandwidth. For these PLL parameters, the MTCS is less than 1 second for a 12 dB-Hz signal. After tightening the bandwidth to 0.4 Hz, the MTCS increase to 60 seconds. While this is an improvement, the MTCS is still very short and carrier tracking is not reliable. However, if the averaging time is increased from 1 ms to 60 ms, the PLL is able to track over 1000 seconds. These simulation results show the limitation of tightening the bandwidth, and motivate the need to increase coherent averaging time to meaningfully increase the MTCS.

This validates the DO metric, which suggests that increasing coherent averaging time is more beneficial to carrier tracking performance in the presence of interference than tightening the bandwidth alone. This is in contrast to the phase jitter metric, which suggests the opposite, that tightening the bandwidth would be more beneficial than extending averaging time.

B. Lower down threshold of σ_ϵ

Section III-B motivated the need for a reduced DO metric threshold, using 22.5 degrees as an illustrating example. And, Figure 5 showed that a reduced threshold on the DO standard deviation would result in a more favorable DO distribution. However, the relationship between the DO distribution and carrier tracking performance still needs to be quantified. In this section, we quantitatively show the relationship between DO standard deviation σ_ϵ (DO distribution) and MTCS (tracking performance).

In section III, we have shown that the inverse-tangent discriminator is completely saturated when the standard deviation of its output reaches 52 degrees. This saturated condition correspond to a 1 ms averaging time and 15 Hz bandwidth

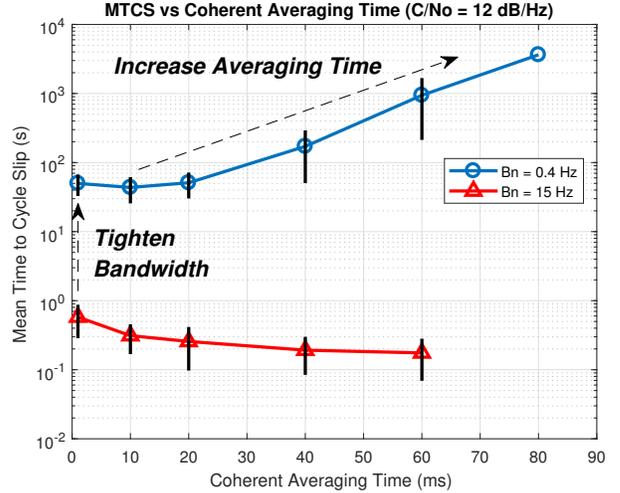


Fig. 6. Mean time to cycle slip versus averaging time for different bandwidths

in Figure 6. This simulation point had a MTCS less than 1 second.

Seeking longer MTCS requires the DO metric threshold, R , to be lowered. To quantify the threshold required for a given MTCS requirement, a relationship between σ_ϵ and MTCS is needed. This relationship is determined using non-linear PLL simulation.

Figure 7 shows the MTCS versus σ_ϵ for a 20 ms averaging time and bandwidth of 0.4 Hz. As the carrier-to-noise ratio is decreased, σ_ϵ increases, and the MTCS decreases. When σ_ϵ reaches 52 degrees the MTCS is less than 30 seconds, which corresponds to DO saturation. Given a MTCS requirement for a GPS application, the goal is to be able to use a figure such as Figure 7 to determine the required threshold necessary for equation 13. Equation 8 can then be substituted into equation 13 to solve for the necessary PLL bandwidth and averaging time.

Generating results for long MTCS can be time-consuming. The longest MTCS shown in Figure 7 is about 600 seconds (10 minutes). To increase its usefulness in PLL design, additional data points corresponding to σ_ϵ less than 44 degrees must be included in Figure 7. In addition, it is necessary to verify that the curve in Figure 7 is invariant under different PLL parameters.

V. CONCLUSION

In this paper, we develop a performance measure for GPS receiver phase lock loops (PLLs) that are subjected to wide-band radio frequency interference (RFI). This technique allows PLL design parameters to be determined given requirements for mean time to cycle slip (MTCS). The methodology is directly applicable to both stationary GPS reference receivers as well as moving receivers.

Using direct non-linear PLL simulation, the PLL performance metric based on the DO standard deviation is verified using MTCS results. These results show the limitation of

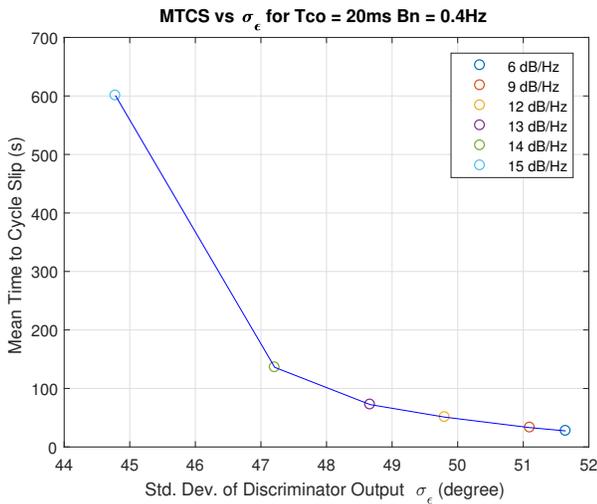


Fig. 7. Mean time to cycle slip versus standard deviation of discriminator output

tightening the bandwidth, and motivate the need to increase coherent averaging time to meaningfully increase the MTCS. This is in contrast to the phase jitter metric, which suggests the opposite, that tightening the bandwidth would be more beneficial than extending averaging time.

PLL simulation was also used to quantify the relationship between the MTCS and DO standard deviation. This relationship can be used as a design guide in choosing a suitable DO metric threshold given a MTCS requirement.

In future work, the results in Figure 7 will be extended to much longer MTCS (corresponding to σ_ϵ less than 44 degrees) in order to increase the usefulness of this figure for practical PLL design. In addition, it is necessary to verify that the relationship between the MTCS and DO standard deviation is invariant under different PLL parameters.

ACKNOWLEDGMENT

We would like to thank our sponsors at the Federal Aviation Administration (FAA) for supporting this research. The views and opinions expressed in this paper are those of the authors and do not necessarily reflect those of any other organization or person.

REFERENCES

- [1] Stevanovic, S., and Pervan, B. A GPS Phase-Locked Loop Performance Metric Based on the Phase Discriminator Output. *Sensors* 2018.
- [2] Pullen, S., and Gao, G. *GNSS Jamming in the Name of Privacy: Potential Threat to GPS Aviation*; Inside GNSS Magazine: Vol. 7 No. 2, March/April 2012.
- [3] Stevanovic, S. Joerger, M. Khanafseh, S. Pervan, B. Atomic Clock Aided Receiver for Improved GPS Signal Tracking in the Presence of Wideband Interference. In Proceedings of the 28th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2015), Tampa, FL, USA, 14–18 September 2015.
- [4] Chan, F.-C., Joerger, M., Khanafseh, S., Pervan, B., and Jakubov, O. Performance Analysis and Experimental Validation of Broadband Interference Mitigation Using an Atomic Clock-Aided GPS Receiver. In Proceedings of the 26th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2013), Nashville, TN, USA, 16–20 September 2013; pp. 1371–1379.

- [5] Razavi, A., Gebre-Egziabher, D., and Akos, D.M. Carrier Loop Architectures for Tracking Weak GPS Signals. *IEEE Trans. Aerosp. Electron. Syst.* **2008**, *44*, 697–710.
- [6] Tsujii, T., Fujiwara, T., Kubota, T. Improvement of INS-Aided GPS Tracking Performance under Strong Ionospheric Scintillation. *Navigation* **2015**, *62*, 111–119.
- [7] Kaplan, E.D., and Hegarty, C.J. *Understanding GPS: Principles and Applications*, 2nd ed.; Artech House: London, UK; Norwood, MA, USA, 2006.
- [8] Borre, K., Akos, D.M., Bertelsen, N., Rinder, P., Jensen, S.H. *A Software-Defined GPS and Glonass Receiver*, BirkhauserBoston: New York, NY, USA, 2007
- [9] Misra, P. and Enge, P. *Global Positioning System: Signals, Measurements and Performance*; Ganga-Jamuna Press: Lincoln, MA, USA, 2006.
- [10] Gardner, F.M. *Phaselock Techniques*, 3rd ed., John Wiley and Sons: Hoboken, NJ, USA, 2005.
- [11] Stevanovic, S., and Pervan, B. Atomic Clock Aided Receiver for Improved GPS Signal Tracking in the Presence of Wideband Interference. In Proceedings of the 28th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS+ 2015), Tampa, FL, USA, 14–18 September 2015.
- [12] Borio, D., and Lachapelle, G. A non-coherent architecture for GNSS digital tracking loops. *Telecommun.* **2009**, *64*: 601..